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PSOC Based Speed Control of BLDC Motor

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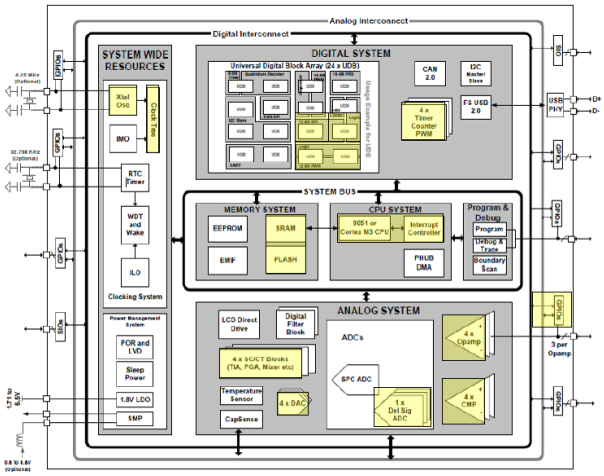
***Abstract*— The traditional brushed DC motors are now replaced by brushless DC motor because of it's higher reliability, efficiency & lower noise. The implementation of Sensored BLDC motor control, using Hall Effect sensors, with speed control using the CY8CKIT-050PSoC@5 device. Hardware over current protection and speed control in the BLDC application is also explained.**

[1] INTRODUCTION

PSOC 5 INTRODUCTION

The CY8CKIT-050 device is in the PSoC 5 family. A block diagram of the device is shown in Figure 2 with the blocks used in the BLDC application highlighted.



DIGITAL SUBSYSTEM

The PSoC 5 digital subsystem provides unique configurability of functions and interconnects. The subsystem connects digital signals from any peripheral to any pin through the digital system interconnect (DSI). It also provides functional flexibility through an array of small, fast, low power universal digital blocks (UDBs) and small blocks targeted to specific fixed functions.

UDBs

- For optimal flexibility, each UDB contains several components:
- ALU based 8-bit data path
- Two fine grained PLDs
- Control and Status Module
- Clock and Reset Module
- A PSoC 5 device contains an array of up to 64 UDBs.
- Flexible routing through the UDB array.
- Portions of UDBs can be shared or chained to enable larger functions.
- Flexible implementation of multiple digital functions, including but not limited to timers, counters, PWM (with dead band generator), UART, I2C, SPI, and CRC generation/checking.
- Fixed function timer blocks in PSoC 5 devices are of 16 bits and configurable to act as timers or PWM that play important roles in embedded systems. PSoC 5 provides up to four instances of the Timer block. If additional Timer blocks are required, they are configured in the UDBs. Timer blocks have various clock sources and are connected to the general-purpose input/output (GPIO) though the DSI.

Configurable digital functional blocks are also available for other specific functions.

ANALOG SUBSYSTEM

The PSoC 5 analog subsystem provides the device, the second half of its unique configurability. All analog performance is based on a highly accurate absolute voltage reference with less than 0.2% error over temperature and voltage. The configurable analog subsystem includes analog muxes, comparators, analog mixers, opamps, voltage references, analog-to-digital converters (ADC), digital-to-analog converters (DAC), and digital filter blocks (DFB). All GPIO pins can route analog signals into and out of the device, using the internal analog bus. This feature enables the device to interface up to 62 discrete analog signals.

THE ANALOG SYSTEM ON THE CY8CKIT-050PSOC@5 DEVICE CONTAINS:

- Four continuous time/switched capacitor building blocks, which can be used to make programmable gain

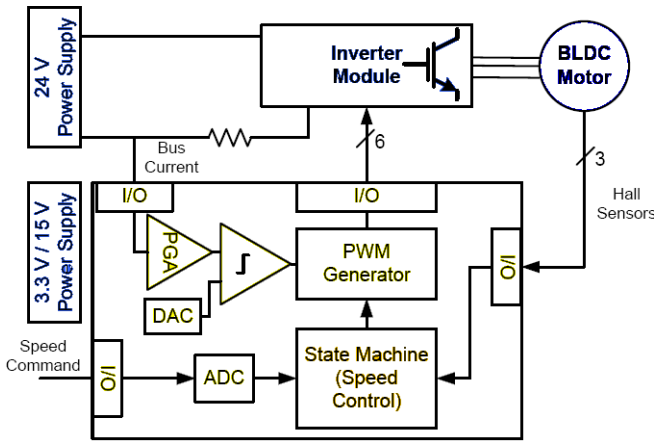
amplifiers (PGA), transimpedence amplifiers (TIA), mixers, and more.

- Four comparators with user configurable speed, accuracy, and hysteresis settings.
- Four dedicated opamps, which can be used as an analog buffer to drive external loads, analog filters, peak detector, a slow comparator, and so on.
- Four DACs, configurable as current or voltage output, which are user configurable output range, direction, power, and speed.
- Delta-Sigma ADC with selectable resolution from 8 to 20 bits. These have user configurable input range, reference, sample rate, and operating mode.

BLDC MOTOR CONTROL BASED ON PSOC 5

The block diagram of the BLDC motor control based on PSoC 5 is shown in Figure 3 and the PSoC Creator™ schematic is shown in Figure 4.

Figure 3. Block Diagram of PSoC 5 BLDC Motor Controller

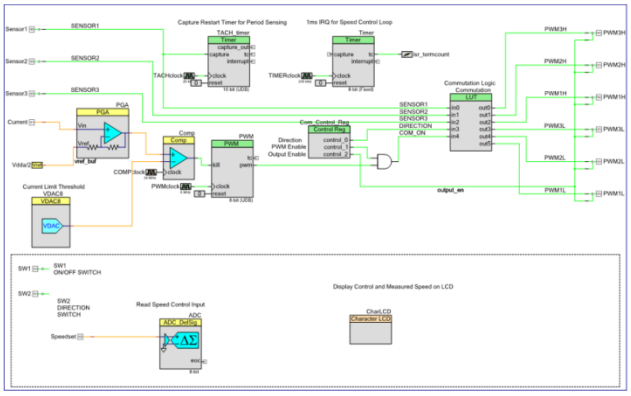


BLDCMotorPWM GeneratorState Machine (Speed Control)I/OI/OADCI/OPGADAC3Hall Sensors624 VPower SupplyI/OPSoC3SpeedCommand3.3 V / 15 VPower SupplyBus CurrentInverterModule
Input control signals to the PSoC 5 are:

- Speed command: Analog input pin that measures the voltage across a potentiometer to set the desired speed of rotation (one analog input pin).
- Motor current detection: Analog input pin to detect and cut off power device driver to protect motor when over current condition is detected (see following section) (one analog input pin).
- Hall Sensors: Three digital input pins connected to the outputs of the hall sensors from the motor. These sensor inputs provide the position of motor and are used to control the commutation by varying the PWM output signals to the power driver (three digital input pins).
- Direction control: Digital input connected to a switch to control the motor rotation between clockwise and counter-clockwise (one digital input pin).
- Start/stop control: Digital input connected to a switch to start and stop rotation of the motor (one digital input pin).

Outputs from PSoC 5 are power device driver signals.

- PWM signals to the high side of the power device driver (three digital output pins).
- PWM signals to the low side of the power device driver (three digital output pins).



The three Hall Effect sensors are fed into a lookup table (LUT), which is created using the PLD capabilities of the UDB, and uses the data from the sensors to determine the motor position. The LUTs programmed logic will then pass the appropriate PWM signals to the GPIO at the proper time. The GPIO pins are connected to a external power driver module which will directly drive the BLDC motor by gating the high voltage supply. The LUT will also control the direction of the motor and control the starting and stopping of the motor based on what is read by the LUT from Com_Control_Reg. This digital logic will work together to produce the commutation sequence to turn the motor as seen in Figure 1.
Speed control is accomplished by reading a potentiometer from an analog input pin with the DelSig ADC. Every time isr_termcount triggers, the firmware will check the ADC and see if any changes to the motor speed are required based on the voltage measured. The current speed of the motor is measured with TACH_timer, which is a 16 bit timer. Once a falling edge of Sensor 1 occurs, we know that the motor has made a complete revolution. This rising edge will trigger a capture on the timer and move the current timer value to a

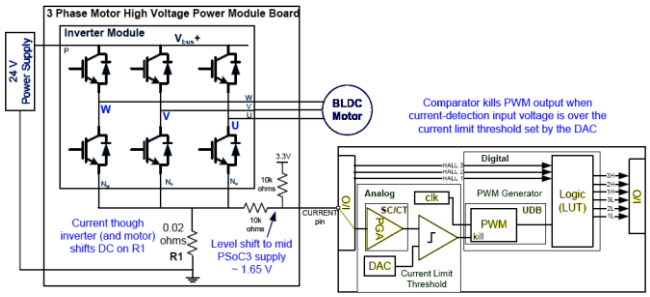
register which we can then read and determine the current motor speed. The calculated motor speed will then be fed into a control loop to compare the measured and expected motor speed. Based on this calculation, the duty cycle of the PWM may be adjusted to more accurately match the desired motor speed.

This design also implements hardware based over current protection which is explained in greater detail in the next section. The comparator output of the over current detection system is tied directly to the PWM kill signal. When over current triggers, the PWM output is killed which will stop all control signals to the external driver module. This will occur regardless of the current CPU process or state.

Over Current Protection

This is implemented in hardware on the PSoC 5. The block diagram is shown in Figure 5.

Figure 5. Over Current Protection Block Diagram for Three Phase Motor High Voltage Power Module Board and PSoC 5



PSoC 5 resources used in the BLDC over current protection are:

- Continuous time (SC/CT) block to implement the PGA.
- Analog comparator – This is a dedicated analog resource and does not use a SC/CT block.
- 8-bit PWM implemented in UDB (The same PWM used to control power device driver) – The output of the comparator triggers the kill input to the PWM when an over current condition is detected.
- Analog buffer, using one of the dedicated analog opamps. (This could be replaced with external resistor dividers and an analog input pin to reduce resource usage).
- VDAC8 – Built in 8-bit voltage DAC, this is used to set the current limit threshold for the comparator. (This could be replaced with external resistor dividers and an analog input pin to reduce resource usage).

To configure over current protection for a desired current limit, values must be selected for the resistor and the current limit threshold. The value of the over current detection shunt resistor is a tradeoff between headroom for the motor operation and robustness of the detection blocks. For a given current limit, enough change in voltage must be generated by the motor current to accurately detect the change with the comparator. However, increasing the resistor increases the ground voltage of the inverter and reduces the headroom to drive the motor.

The current limit threshold and resistor value are related by the following equations, where gain is the gain of the PGA, Current is the desired limit, and vref is the level shifted reference voltage.

Introduction to BLDC motor

BLDC motors are more efficient than brushed DC motors. For the same input power, a BLDC motor converts more electrical power into mechanical power than a brushed motor because of the absence of friction due to brushes. In a brushed motor design, the brushes are used to change the poles of the electromagnet in order to keep the motor spinning. Due to this lack of brushes, there is nothing to mechanically handle the polarity changes. As a result, an electronic controller is required to continuously switch the phase of the winding which will keep the motor spinning. To do this, the stator windings are energized in a particular sequence as seen in Figure 1. BLDC motors have three phases. With this topology, to move the motor, two phases are driven during each commutation cycle. One phase is driven high (VMotor) and the other is driven low (GND). The remaining phase is left floating. With every commutation step, the motor will move 60 degrees. Upon completion of all cycles, the motor will have moved a complete 360 degrees.

To implement this sequence, it is important to know the rotor position. This is done by using sensors, such as Hall Effect sensors (sensored control), or by sensing back EMF(sensorless control). Hall Effect sensors are embedded in the stator. When the rotor magnetic poles pass near the hall sensors, they supply a high or low signal, indicating that the north or south poles are passing nearby. The position of the rotor is derived from the exact combination of the three hall sensor signals.

Summary

Cypress BLDC motor control with PSoC 5 incorporates over current protection and closed loop speed control for an optimized solution. Over current protection, which is very important in BLDC control to avoid over current damage, is implemented with on-chip hardware. The PSoC 5 BLDC motor control solution has low total system cost and leaves significant PSoC 5 resources available for additional system functions.

References

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