Partially Adaptive Cluster Based Routing for Network-on-Chip

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***Abstract* – As the technology is scaling, reducing wire delays is the major hurdle in increasing communication speed between the cores of System-on-Chip (SoC). Also in today's technology 50% of silicon area is occupied by interconnects. Efficient use of interconnects is possible due to highly scalable and reliable Network-on-Chip (NoC) communication architecture which has replaced long buses by routers. Routers in NoC make use of intelligent routing algorithms to route the information reliably between the cores irrespective of the topology used. With the help of routing algorithms router optimizes the use of interconnects. Algorithms should provide deadlock free and congestion free routing while ensuring the reachability to destination. This paper presents partially adaptive Cluster based routing referred to as Cluster based routing for regular mesh topology which, (i) Uses cluster approach to reduce the size of routing table. For a 8x8 Mesh there is 76.57% area reduction in routing table. (ii) Provides deadlock free partially adaptive algorithm without use of virtual channels which is achieved by avoiding cyclic paths. (iii) Uses adaptivity to avoid congestion by uniform distribution of traffic between cores.**

Index Terms – Cluster, routing, NoC.

I. Introduction

With the advent of new VLSI technology System-on-Chip (SoC) concept is the current trend. It reduces the interconnection length between the cores as compared to System-in-Package resulting in reduction of communication delay. Thus we are able to achieve SoC's operating at much higher frequencies but up to a certain extent. Adding more and more functionality on a single chip, number of interconnect and its length is going on increasing. Estimate is that about 50% of chip area is occupied by interconnects. Due to technology scaling all parameters of the device scale down linearly but the wire resistance is increasing because of area reduction and non scalability of interconnection length. Network-on-Chip (NoC) provides a platform to make efficient use of interconnects by replacing buses by routers. NoC is generally described by topology, switching technique

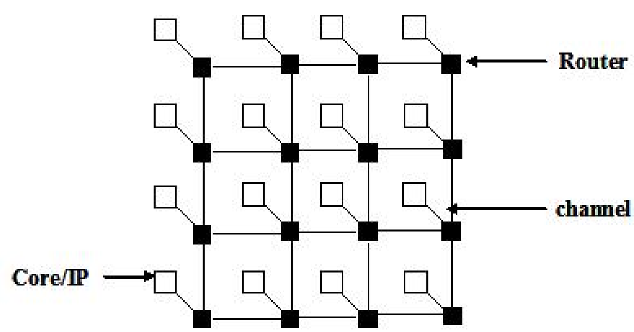


Fig. 1 Mesh topology

and routing mechanism. Noc architecture consist of routers connected to the cores by network interface as well as to adjacent routers by physical channels.

A. Topology

Cores, network interface and router together forms a tile. The arrangement of tiles and their connectivity results in to topology. Various NoC topologies are Mesh, Torus, Butterfly, Ring, Spidergone, etc. Due to simplicity in structure and high scalability mesh topology is widely used. 4x4 Mesh Topology is shown in Fig.1. Each router has five input and five output ports. Four ports for four directions East, North, South and West and fifth port for core (Processing Element). Each incoming message is divided into packets and packets are further divided into flits (flow control unit). These incoming flits are stored into input buffers. If multiple input ports are requesting to send data onto same port the arbiter helps in resolving such request. Depending upon the arbitration result crossbar switch connects an input port to a requested output port. The basic and minimum required architecture of the router is shown in Fig. 2.

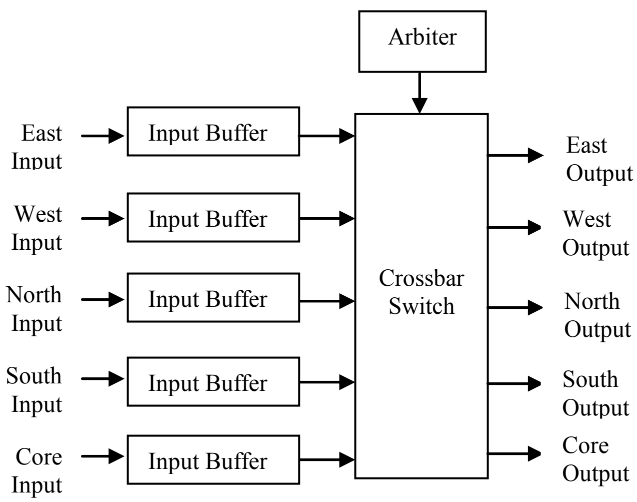


Fig. 2 Architecture of Router

B. Switching Technique

Switching techniques determine how the crossbar switch connects the router's input to output and the time at which flits may be transferred along the channels. Basic switching techniques are circuit switching, packet switching, virtual-cut-through switching and wormhole switching.

1) Circuit Switching: In this technique a physical path from source to destination is created and reserved prior to transmission of flits. Complete message is transmitted at full bandwidth of the hardware path. Once the channel is reserved other routers cannot use it for communication. Channel sharing is not possible.

2)Packet Switching: The messages are partitioned and transmitted as fixed length flits. Each flit is routed from source to destination. A packet is completely buffered at each intermediate node before it is forwarded to the next node. Thus this technique is also referred to as store and forward switching technique. Buffer space requirement is more in this technique

3) Virtual-cut-through Switching: Rather than waiting for the entire packet to be received, the packet header can be examined as soon as it is received. The router can start forwarding the header following the data flits as soon as routing decision is made and when output buffer is free. The entire message need not be buffered at the input and can be passed to the input of the router before the complete packet is received at the current router. If the header is blocked on a busy output channel, the complete packet is then buffered at that node. At this instance it resembles packet switching. This approach reduces latency but the buffer requirement is large same as packet switching.

4) Wormhole Switching: To design compact routers buffers used inside routers should be very less in number and of small size. Therefore message packets are further divided into smaller sizes called flits. The size of buffer is now size of flit. As soon as the router receives a flit it forwards to the next potential router node till all the flits reach the destination. In case if the header flit gets blocked then the flits of one message are buffered at whichever node they are present. So during blocking, then entire message is not stored at one particular node. Thus the message is spread through out the network. Advantage of this technique is less buffer space required as compared to other switching techniques. We are using wormhole routing technique because it occupies less buffer space.

C. Routing Mechanism

Routing mechanism determines the actual path of the message from one router to other. Various routing mechanisms are deterministic routing and adaptive routing. Adaptive routing can be partially adaptive or fully adaptive.

Widely used deterministic routing is XY routing because of its simplicity and easy to implement. XY routing first takes path in X direction till it reaches its destination column Y and then travels Y direction till the destination is reached. It is deadlock free but every time it takes same path to reach same source and destination pair and therefore this routing leads to congestion and hotspots. To avoid congestion adaptive routing algorithms are used in which with the help of routing table it determines path from source to destination. Fully adaptive routing algorithm provides routing in all directions thus allowing uniform distribution of traffic but this might lead to cyclic paths resulting into livelock. Partially adaptive algorithms analyse the traffic pattern of the network and accordingly switch between adaptive and deterministic.

We have proposed and implemented partially adaptive Cluster based routing algorithm. Section III explains our proposed algorithm and section IV shows the result of execution of our algorithm which is written in C.

II. Overview Of Routing Algorithm

The routing scheme DyAD (Dynamically Adaptive and Deterministic) [1], [4] is combination of deterministic XY routing and adaptive odd-even routing. Depending upon congestion threshold, routing switches between deterministic and adaptive. But congestion threshold is based on local traffic.

Q routing algorithm [2] is a distributed routing algorithm in which each router tries to minimized estimated cost involved in routing packets to its destination. By referring routing table router routes flits from source to destination via its potential neighbor which has low cost. Cost is in terms of time taken by the flit to reach destination. This algorithm takes care of faulty links as well as congested links by penalizing the path cost. This algorithm is fully adaptive and thus can enter livelock. It is suggested to use virtual channels to avoid livelock and deadlock [8]. But virtual channels will increase silicon area. XY deterministic routing [6] is faster initially than any other partially or fully adaptive routing algorithms but it cannot explore different paths even if they are available to reach destination. One fixed path may lead to hotspot and congestion.

Turn model based algorithms like West first, North last, Negative first [6] are deadlock and livelock free routing algorithms for mesh topology networks. In this method packets take minimum number of turns avoiding cyclic paths. But the degree of adaptiveness is uneven [10]. Odd-even turn model provides more degree of routing adaptivity as compared to above turn models [10].

III. Proposed Algorithm

Cluster based routing algorithm is partially adaptive which prevents deadlock and without use of virtual channels. It maintains global information about faulty and congested links. Routing table (RT) contains the information about the cost to reach destination from the source via one of the neighbors of the source. Cost is in terms of number of times a flit has passed through the adjacent nodes. Routing table required at each node is shown in Fig. 3. In Cluster based routing, cluster approach reduces the size of routing table as shown in TABLE I.

N: Total number of nodes in mesh, Y: number of neighbor nodes and C: Number of clusters. D: Total number of destinations in one cluster and is given by D = (N/C). To avoid cyclic path adaptability is allowed in East, West and South direction in our algorithm. This reduces the size of RT further in terms of columns.

$$AreaUtilized = \frac{RT size of proposed Cluster based algorithm}{RT size of Q routing algorithm}$$

$$AreaUtilized = \frac{\left(\frac{N}{C} + C\right)(Y - 1)}{N * Y}$$

$$AreaUtilized(\%) = \left(\frac{1}{C} + \frac{C}{N}\right) * \left(1 - \frac{1}{Y}\right) * 100 \qquad (1)$$

Thus,

$$Area\ Reduction(\%) = 100 - AreaUtilized(\%)$$

Consider the mesh for N=64 nodes, and each node has Y = 4 neighbours as shown in Fig. 4. Without cluster approach size of the RT required for each node is 64x4, which is used in Q-routing [4]. Using cluster approach RT for each node is (16+4)x3. Thus gain achieved in terms of area for the routing table is 23.43% or reduction in area is 76.57% from Equation (1).

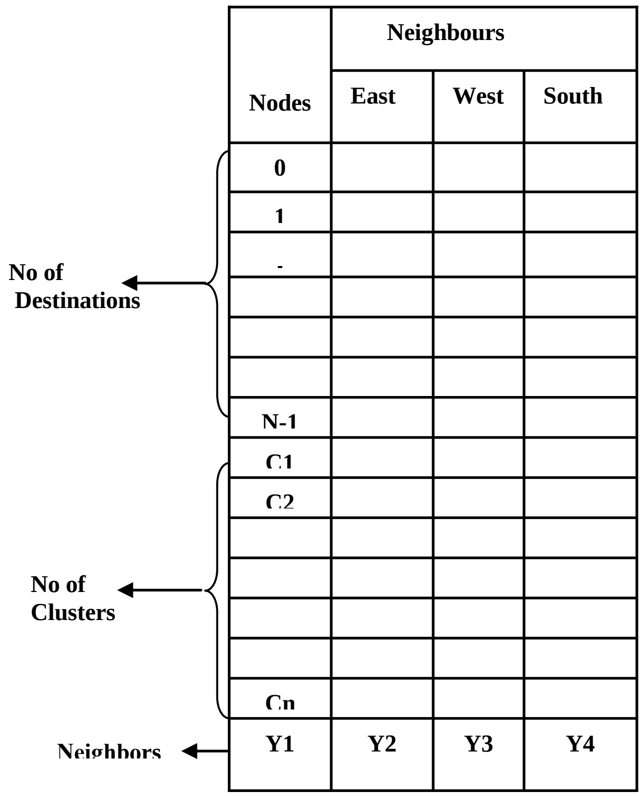


Fig. 3 Routing table (RT) at each node

TABLE I
SIZE OF ROUTING TABLE

	Q routing	Partially adaptive Cluster based routing
Size of routing table (RT)	N x Y	((N/C) + C) x (Y - 1)

A. Routing Criterion

Cluster based routing algorithm uses combination of deterministic XY and partially adaptive routing. Depending upon the location of source and destination node it will perform either deterministic XY routing or partially adaptive routing and routing in East, West and South are only allowed to prevent deadlock.

According to the X and Y axis notations shown in Fig 4. every node will have its cluster address and own address. Addresses on X and Y axis are inter cluster addresses while addresses written inside the cluster represents each node's own address called Intra cluster address. Irrespective of the inter or intra cluster communication if destination node's Y axis address is less than or equal to source node Y axis address then perform deterministic XY routing, else perform partially adaptive routing. In partially adaptive routing North direction is restricted to remove cyclic paths for prevention of deadlock.

Fig. 4. Cluster and node addresses

B.. Cluster Based Routing Algorithm

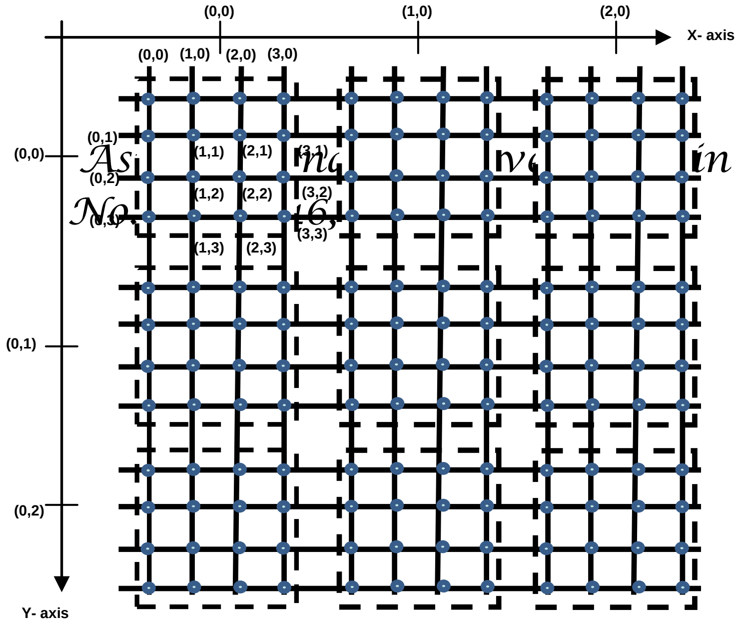
Every node has cluster address and its own address. First current cluster address is compared with destination cluster address to reach destination cluster. After reaching destination cluster, current node address is compared with destination node address to reach the destination node. Following notations are used for representation of different terms.

Sc = Source cluster.
Dc = Destination cluster.
Src = Source node.
Dest = Destination node.
q = Link cost which is number of flit traversals between two adjacent nodes.
Y = Selected neighbour node
Ssc(Dc,Y) = cost to reach destination cluster from source cluster via neighbour
Ssrc(Dest,Y) = estimated cost to reach from source to destination cluster from source via source's neighbour
YDc = Y axis address of destination cluster
YSc = Y axis address of source cluster
YDest = Y axis address of destination node
YSrc = Y axis address of source node

1) Initialize all link cost for all nodes
2) Initialize estimated cost for all nodes

$$Ssc(Dc,Y) = 0$$
$$Src(Dest,Y) = 0$$

3) If source node cluster is not equal to destination Node cluster then
   a) If YDc < YSc do deterministic XY routing
   b) If YDc $\geq$ YSc do partially adaptive routing
      i) Generate a random number



$r \in \{0, n\}$ -----(A)

ii) If $r \leq \in$ then choose a random neighbour of the current source node to go to destination cluster else

iii) Choose a neighbour which has a minimum cost from the routing table.

iv) Chosen neighbour node sends its cost to reach destination back to its current source node.

v) If the cost is received in estimated time 't' then the cost is updated in the routing table of the current source node (Ssc = (1-α)Ssc + αq) else

vi) Cost is penalized and updated in the routing table (Ssc = penalty + q).

vii) If it is not a final destination cluster then repeat steps from (A)

4) When destination cluster is reached then

a) If YDest < YSrc do deterministic XY Routing inside destination cluster.

b) If YDest ≥ YSrc do partially adaptive routing inside destination cluster.

i) Generate a random number

$r \in \{0, n\}$ ----(B)

ii) If $r \leq \in$ then choose a random neighbour of the current source node to go to destination node else

iii) Choose a neighbour which has a minimum cost from the routing table.

iv) Choosen neighbour node sends its cost to reach destination back to its current source node.

v) If the cost is received in estimated time 't' then the cost is updated in the routing table of the current source node (Ssrc = (1-α)Ssrc + αq) else

vi) Penalized cost is updated in the routing table (Ssrc = penalty + q).

vii) If current node is not equal to destination node then repeat steps from (B)

5) When source nodes and destination nodes are the same exit the algorithm.

In Cluster based routing each node is addressed by its own address and its cluster address. Each node has its routing table to store the cost Ssc and Ssrc to reach the destination cluster and after reaching destination cluster to destination node. Link cost between two neighbouring nodes denoted by q increments every time for flit traversal. By using combination of deterministic XY and partially adaptive algorithm flit travels from source node to destination node. To prevent deadlock and livelock north direction is restricted.

After initializing the routing table,to reach destination cluster from source cluster first Y address of destination cluster is checked with the source cluster. If Y address of destination cluster is less than the source cluster's Y address then XY routing is performed otherwise partially adaptive routing will be performed. In partially adaptive routing first random number is generated in particular range. If random number is less than epsilon ($r \leq \in$) then source node randomly selects one of its neighbour to route the flit to reach the destination cluster otherwise it will choose neighbour which has minimum cost to reach destination cluster. After selecting neighbour if neighbour does not send its cost to reach destination cluster within estimated time to its source or current node, for that node cost is penalized and updated in current node's routing table. Thus penalizing cost takes care of faulty links. If neighbour sends cost in reasonable time then flit will be routed successfully from current node to neighbour node. Now neighbour node will become current node and it will choose the neighbour node either randomly or by minimum cost to reach destination cluster this process repeats until the filt reaches the destination cluster.

As destination cluster is reached if Y address of destination node is less than the Y address of current node then it will perform XY routing otherwise partially adaptive routing. In partially adaptive routing it will follow the same procedure as to reach destination cluster now difference is instead of cluster it has to reached destination node by selecting neighbour node either by randomly or by minimum approach. In this algorithm every time we are making current node as a source node. When address of source becomes equal to address of destination the message routed successfully from initial source node to the destination node.

IV. RESULT

Cluster based routing algorithm's logic have successfully implemented using C programming. Refer Fig. 5. to view the result.

V. CONCLUSION

Partially adaptive Cluster based routing referred to as Cluster based routing uses cluster approach to reduce the size of routing table. Deterministic XY and adaptive routing is used. In adaptive routing north direction is restricted to avoid cyclic paths preventing livelock and deadlock. Due to this, for a 8x8 Mesh there is 76.57% area reduction in routing table.

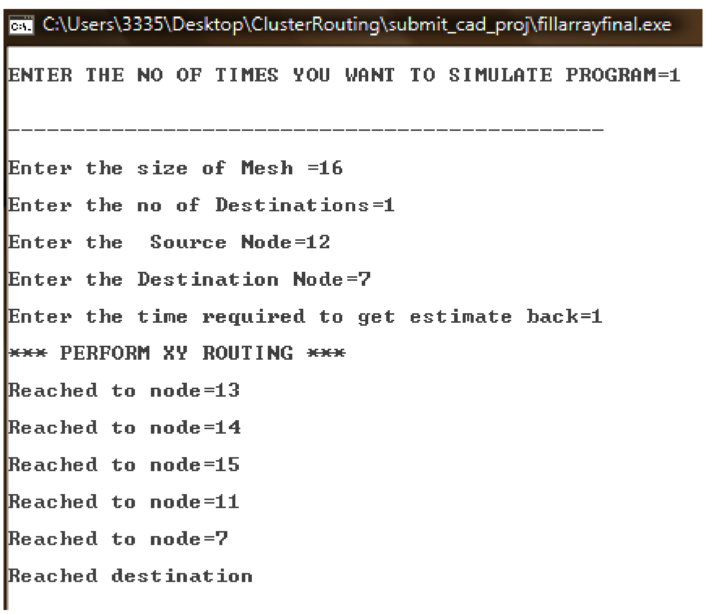


Fig. 5 Routing result

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REFERENCES

[1] David Atienza, Federico Angiolini, Srinivasan Murali, Antonio Pullini, Luca Benini, Giovanni De Micheli, Network-on Chip Design and Synthesis Outlook, Elsevier Science, November 2007.

[2] Rickard Holsmark, Maurizio Palesi, Shashi Kumar,Deadlock free routing algorithm for irregular mesh topology NoC systems with \ rectangular regions, Journal of Systems Architecture 54(2008) 427-440.

[3] Jingcao Hu and Radu Marculescu,DyAD - Smart Routing for Netwoks-on-Chip, CSSI Technical Report,USA.

[4] R.Narasimhan, Ujjwal Kumar, B.Ravindran, Vijay Laxmi, M.S.Gaur, and B.M.Al Hashimi,Application of Q-Routing Algorithm in Networks on Chip.

[5] Jose Duato, A New Theory of Deadlock-Free Adaptive Routing in Wormwhole Networks, IEEE Transactions on Parallel and Distributed Systems, vol 4, No.12 December 1993.

[6] Christopher J.Glass and Lionel M.Ni,The Turn Model for Adaptive Routing, Association for Computing Machinery, 1992.

[7] Alien Vieira de Mello, Luciano Copello Ost, Fernando Gehm Moraes,Ney Laert Vilar Calazans,Evaluation of Routing Algorithms on Mesh Based NoCs, Technical Report Series No.040, May,2004.

[8] Zhaohui Song, Guangsheng Ma, Dalei Song,A NoC-Based High Performance Deadlock Avoidance Routing Algorithm.

[9] Everton Alceu Carara, Fernando Gehm Moraes,Deadlock-Free Multicast Routing Algorithm for Wormhole-Switched Mesh Networks-on-Chip, IEEE Computer Society Annual Symposium on VLSI, 2008.

[10] Ge-Ming Chiu,The Odd-Even Turn Model for Adaptive Routing, IEEE Transactions on Parallel and Distributed Systems, vol 11, No 7, July 2000.