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System Level Modeling and Simulation of Built-in-Self-Test Enable Oversampling Analog-to-Digital Converter

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***Abstract*— System-level modeling is generally needed due to simultaneous increase in design complexity with multi-million gate designs in today's system-on-chips (SoCs). SystemC is generally applied to system-level modeling of Sigma-Delta ADC. CORDIC technique and test generation for the testing of mixed signal circuit components such as analog-to-digital converter is mostly implemented in system level modeling. This work focuses on developing fast and yet accurate model of BIST approach for Sigma-Delta ADC. The Sigma-Delta modulator's ADC static parameters as well as dynamic parameters are degraded. One of the dynamic parameters, signal-to-noise ratio (SNR) is directly obtained by the SIMSIDES (MATLAB SIMULINK tool). Then, the obtained parameters are tested by using Built-in-self-test that is desirable for the VLSI system in order to reduce the non-recurring cost (NRE) per chip by the manufacturer. This paper demonstrates a possibility to realize a simulation of testing strategy of high-resolution Sigma-Delta modulator using MATLAB SIMULINK and Xilinx EDA tool environment. This work also contributes towards the Output Response Analyzer (ORA) being used for testing parameters which help in reducing the difficulties in design of the complete ORA circuit. Moreover, the reusable features of hardware in the computation of different parameters are also improved in the ORA design.**

Keywords— ADC; BIST; Output Response Analyzer ;CORDIC ; SNR;TSG.

I. INTRODUCTION

With the increase in functionality of integrated on a single chip is basically a digital-driven trend . In order, to communicate with the outside or say analog world, analog-to-digital (A/D) and digital-to-analog (D/A) converter plays an important role towards the interfacing between analog and digital domains [3]-[5]. Analog-to-digital Converter (ADC) is widely used as a mixed signal device in many of the system-on-chip designs. Now a day, a trend toward integrating the complete mixed signal system onto a single chip is in heights. So with reduced size, cost and power consumption, the promotion towards the development of new generation of electronics systemic accomplishing all major features for the interaction of real time world to the digital processing circuitry is in its great demand.

The task of testing a VLSI chip to guarantee its functionality is exceptionally complex and often very time taking. In addition to the difficulty of testing the chips (IC) themselves, the incorporation of the chips into systems has caused test generation's cost to grow highly. The methodology to deal with the testing problem at the chip level is to incorporate built-in self-test (BIST) capability inside a chip. This increases the controllability and the observability of the chip[5]-[7], In conventional testing, test patterns are produced externally through the help of computer aided design tools(CAD). The test patterns and the expected responses of the Design under test to these test patterns are used by automatic test equipment (ATE) to determine if the actual responses same as the expected ones[29]. On the other hand, in built-in self-test, the test pattern generation and the output response estimation are done on chip; thus, the use of high-end automatic test equipment (ATE) machines to test chips can be avoided [10]-[12].

High-resolution ADCs with high sampling rates are required in a broad area of high-performance applications, such as high-grade imaging systems, wireless communications, and radar [14]-[18]. To deliver ADCs satisfying the requirements of the applications, it is obligatory that they are tested as less time as possible, but without negotiating the quality of the test. The analog to digital converter is the standard of the mixed circuit and this circuit is the most exclusive to test due both to the ADCs standard tests being quite long and to the high price of mixed signal testers and other test instruments [19]-[22]. The use of BIST techniques relieves the dependency on costly test equipment and allows delivering low-cost devices [23]-[26].

A. SIGMA-DELTA CONVERTERS

Sigma delta Modulator based converters operate at oversampling frequency. That means the sampling frequency is much greater than message signal (Fm). Compared with Nyquist rate ADCs, oversampling ADCs gets high resolution in spite of analog components it uses digital signal processing for converting analog-to-digital conversion[27] and due to the oversampling sigma-delta ADCs; they do not required steep roll-off anti-alias filtering, [30]-[32]which is the prime requirement of Nyquist rate ADCs. Thus, higher order with better and higher linearity are no used and generally avoided to clarify why the study was undertaken and what hypotheses were tested[33]-[35]. In earlier research the hardware design of Analog to digital world standardized commonly by languages such as VHDL and Verilog. Lately, there has been a growing interest in alternative languages for coding at a much higher level of abstraction. SystemC, and System-Verilog represent the most widespread language Figure 1. shown below . These languages equipped with well-known syntax with powerful constructs, enabling the realization and simulation of huge complex systems; in specially SystemC has grown up nd become popular[28].

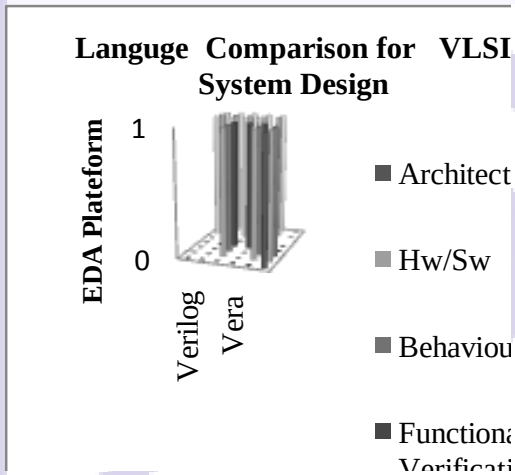

Figure 1. Language Comparison for Hardware Realization

II. BACKGROUND

A. *Polynomial Approximation*

An alternative approach for the approximation of arbitrary function for closed intervals by using polynomial can also be used. However, in this approach pre determination of derivatives are required but is frequently unavailable. Moreover, when the given data are large the calculation for the matrix is very complex as well as a long operating time will be necessary.

B. *CORDIC TECHNIQUE*

The advent of reconfigurable logic of computers permits the higher speed of dedicated hardware solutions at the costs that are competitive with traditional software approach. Even more, the hardware-efficient algorithm is a class of iterative solution for trigonometric and other transcendental functions using only shifts and adds to perform. The trigonometric functions are mainly based on vector rotations, but other functions are implemented by the use of incremental expression based on the desired function. The trigonometric algorithm is called CORDIC (Coordinate Rotation Digital Computer).

Table I. Comparison tables of the above methods

Technique	Cost	Complexity
Maclaurin Series	High	More
Polynomial Approximation	Moderate	More
CORDIC technique	Moderate	Moderate

C. PROBLEM IDENTIFICATION

This section identifies and formalizes the problem faced while implementing the references.

D. Problem Statement:

After reviewed the paper its summarized that there are some limitations in the process taken.
Some of them are –

- BIST technique has not been implemented for the sigma delta obtained from SIMSIDES.
- The value of static parameters & SNR is very less in most of the cases, which is not desired.
- Computational time is more.
- The large memory capacity is required in the circuit.
- Model simulation is not correct due to the non-Linearity.
- On chip overhead area is more.

III PROPOSED METHODOLOGY

The objective of this proposed work is:-

- To design and extract the following parameters of sigma delta modulator:-
  -Offset error
  -Gain error
  -DNL
  -INL
  -SNR
- To test the improved output of a switched capacitor second order sigma delta modulator, designed in SIMSIDES by using CORDIC technique.

A. CIRCUIT UNDER TEST

The circuit under test (CUT) is a second order sigma delta modulator designed by using SIMSIDES. SIMSIDES (SIMULINK-based Sigma-Delta Simulator) is a MATLAB SIMULINK tool having S-function blocks using switched capacitor technique.

B.Output Response Analyzer

The ORA of the BIST system has been designed by using Coordinate Rotation Digital Computer (CORDIC) technique. This technique is applied to establish the sine wave reference histogram on chip with sufficient accuracy.

C. The Basic CORDIC Technique

The CORDIC technique gives an iterative formulation to evaluate many elementary functions, like logarithm, trigonometric function and division, using a shift-and-add approach.

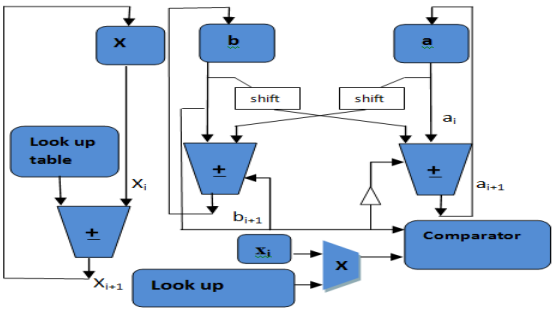

Figure 2: Block diagram of basic CORDIC Technique

D. CODE/COUNTING ASSIGNMENT

- **Code_cnt**: The modulator's output code is captured, analysed and indicated by this counter, viz 0 to 2N-1.
- **Sample_cnt**: Represents the total number of samples for each code. For each code, it counts from 0 to Nt-1.

Table II
Algorithm: Sample_cnt

```
dt = 1/Fs;                % seconds per sample
  StopTime = 1;           % seconds
 N = size(t,1);           %% Sine wave:
Fc = 12;                  % hert
  x = cos(2*pi*Fc*t);
%% Fourier Transform: X = fftshift(fft(x));  %% Frequency
specifications:
  dF = Fs/N;              % hertz
 f = -Fs/2:dF:Fs/2-dF;    % hertz
 %% Plot the spectrum:
 figure;
 plot(f,abs(X)/N);
 xlabel('Frequency (in hertz)');
 title('Magnitude Response');
```

Practical Code Counting

- **Code_sta**: Connected to the modulator's output directly. The practical sine wave histogram of the code is computed using counter. As long as the modulator's output is identical to the present value of the Code_cnt, the counting for number of blocks will be increased. If the value of Code_cnt is changed, this increment will stop.

Table III
Algorithm: Counter [code counting]

```
N=1000;
c=[2 3 5 7];
counter=1;
for x=1:N
   V=mod(x,c);
   F=V(V==0);
   if isempty(F)
      Prime(counter)=x;
     counter=counter+1;
   else
      continue;
   end
end
```

E.CORDIC-based Reference Histogram Calculator

- **Input_set:** A Multiplexer (MUX) which selects the functionality of the CORIC block to perform.
- **CORDIC:** An embedded CORDIC calculator. Functions such as the inverse sine function and division can be calculated.
- **Reg:** We have used two registers to store the intermediate computing values for saving the area overhead. Further, the cost will be reduced as compared to the method using an extra memory.
- **Offset_cal:** The input offset error can be evaluated.Input_cal: Various input parameters are calculated using this block, when the output of Code_cnt is increased.
- **H_ref:** This block is used to evaluate the final value of the sine wave histogram for the code.

Table IV
Algorithm: CORDIC

```
 function [x, y, z] = cordic_rotation_kernel(x, y, z, inpLUT, n)
% Perform CORDIC rotation kernel algorithm for N
iterations.
xtmp = x;
ytmp = y;
for idx = 1:n
```

```
    if z < 0
        z(:) = accumpos(z, inpLUT(idx));
        x(:) = accumpos(x, ytmp);
        y(:) = accumneg(y, xtmp);
    else
        z(:) = accumneg(z, inpLUT(idx));
        x(:) = accumneg(x, ytmp);
        y(:) = accumpos(y, xtmp);
    end
    xtmp = bitsra(x, idx); % bit-shift-right for multiply by 2^(-idx)
    ytmp = bitsra(y, idx); % bit-shift-right for multiply by 2^(-idx)
                                end
```

F. Parameter Evaluating Circuit

- Parameter_out: This block is used to calculate the static parameters of the Sigma-Delta modulator using the output of the Code_cnt, H_ref as well as CORDIC block. The static parameters which can be calculated are offset error, gain error, DNL, INL and Dynamic parameters like SNR.

With the above description the proposed block diagram for the design of ORA for BIST of Sigma Delta Modulator can be given in figure 3.

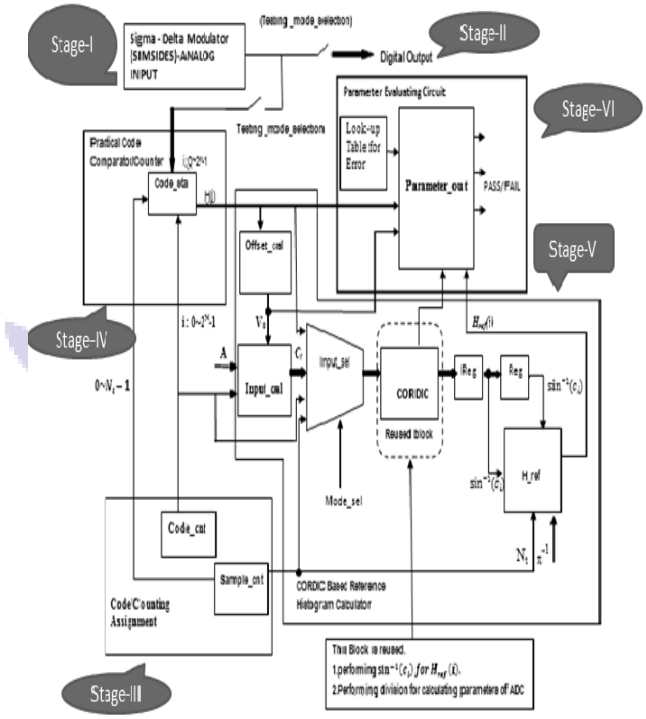

Figure 3. Proposed CORDIC enable ORA for BIST

G. On-Chip Signal Generator On VHDL And Verilog Platform

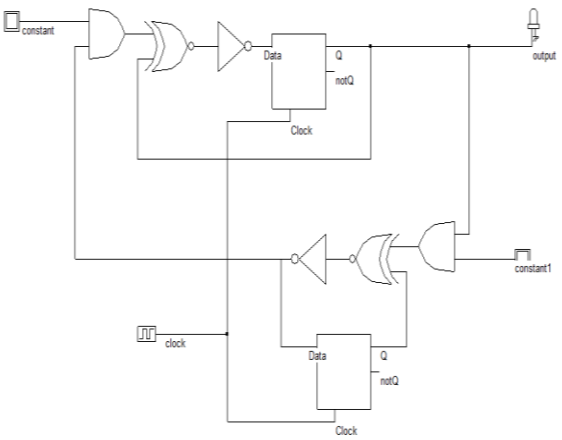

Figure 4. Hardware Gate Level Model Of Test Signal Generator.

III. RESULT AND DISCUSSION

This section presented the experimental setup and the results of the simulated model .This section commences with a discussion of the components required in the experimental setup. The section then presents the result obtained. Finally, concludes by a discussion and analysis of the result obtained by considering required performance indicators like DNL, INL and SNR.

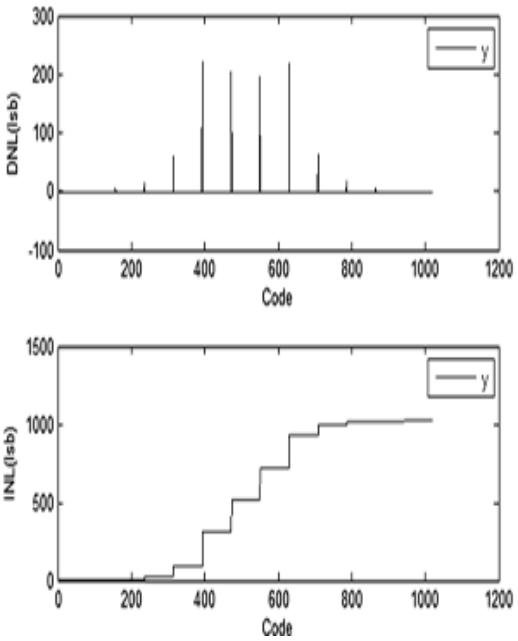

Figure 5. SIMSIDES Computation of INL and DNL

*A. For getting the BIST output***:**

The SIMSIDES output is given to the ORA of the BIST Circuit and the testing parameters are obtained in figure 6.:

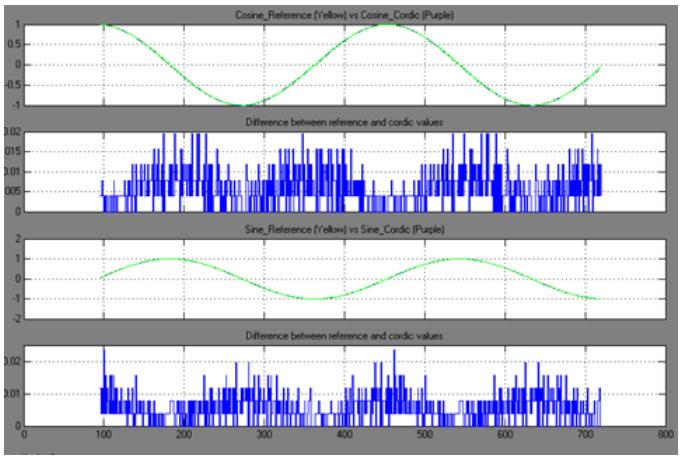

Figure 6. SIMSIDES ORA Response of calculated for Test Pass or Fail

Table V
Comparison Table of Result obtain

S.N.	Parameter	Ref.[3]	Ref.[9]	Ref.[27]	This Work
1	**Language [Accuracy]**	Low	Medium	Medium	**High**
2	**Simulation Speed**	Low	Medium	High	**Very High**
3	**Hardware Complexity**	Very High	Medium	Medium	**Low**
4	**DNL**	< + 0.01 LSB	< + 0.01 LSB	< + 0.01 LSB	**< + 0.01 LSB**
5	**INL**	< + 0.01 LSB	< + 0.01 LSB	< + 0.01 LSB	**< + 0.01 LSB**
6	**SNR**	0.860	0.87	0.92	**0.94**
7	**Data-bit width**	13 bit	13 bit	13 bit	**13 bit**

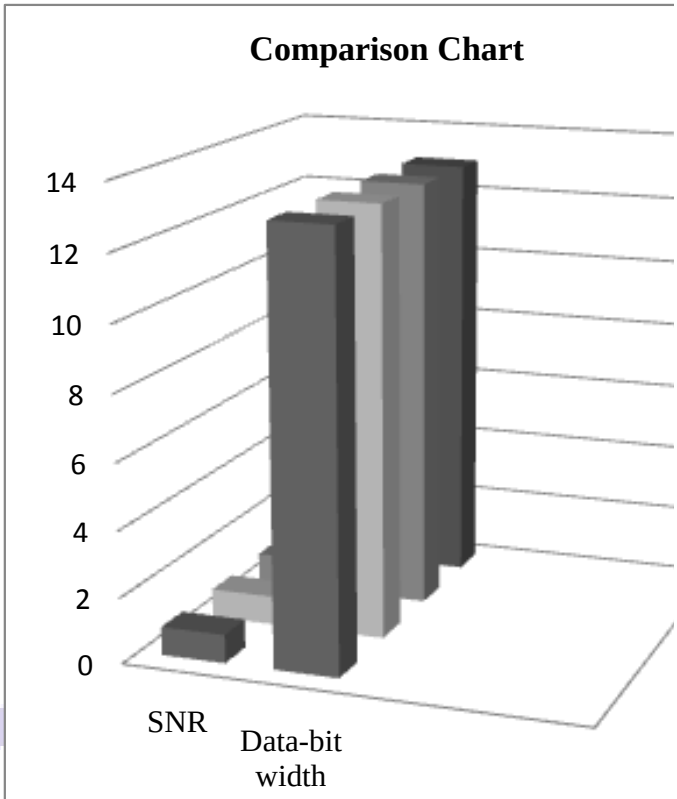

Figure 7. Shows Comparative result

V.CONCLUSION

This can be observed with the help of results and the discussions that the work is area efficient and better performance is resulted with improved the resolution and signal to noise ratio (SNR). Realization of system level Hardware model of BIST with 2nd order low-pass sigma-delta modulator design under test has been achieved.The modulator's static and dynamic parameters i.e. offset error, gain error, DNL, INL and SNR are obtained using sine wave histogram test and are calculated using the proposed ORA circuit.

The parameter errors and hardware cost for the realization purpose are being calculated. Therefore, the accuracy of the proposed technology is considerably high. Since the proposed technology is entirely a digital circuit therefore, the performance of the modulator ORA will not be degraded.

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