DESIGN AND TESTING OF MULTIPLIER CIRCUIT USING BIST FOR FPGA

Siddhesh Bhasale,Tehseen Dadwani,Ankush Nalewad
Department of ECE
MES College of Engg
Pune-411001
siddheshbhasale@gmail.com
tehseendadwani@gmail.com
ankushnalewad@gmail.com

Dr K.S.Tiwari
Associate. Prof, Dept. of ECE,
MES College of Engg
Pune-411001
kanchan.tiwari@mescoepune.org

Abstract—**The intricacies of IC (Integrated circuits) are increasing at a swift pace, Thus testing these ICs for erogenous faults has become very important. BIST is very popular testing mechanism which involves the design of test circuitry around a system that automatically tests the system by applying certain test stimulus and observing the system response generated due to the stimulus of the applied testing patterns. In BIST, the framework for testing the circuit is integrated in the system hardware, As a result the testing process becomes fast and cheaper than using ATE (Automatic test Equipment). Multipliers are basic building blocks of electronic design, they are extensively used in processors, microcontrollers, computers etc for signal processing. The self testing ability of a multiplier is an improvement compared to a basic multiplier design. This feature enables on-field testing of the multipliers without the use of costly ATEs. The BIST (built-in-self-test) functionality gives a brief analysis of the hardware faults that may be present in the multiplier. This paper puts forward a implementation of a multiplier with BIST functionality. Using BIST the multiplier is checked for various stuck at faults. Xilinx Vivado tool is used for modeling of this multiplier. For the design of self-test circuit, TPG (Test Pattern Generator) is used.**

Keywords— Built-In-Self-Test, BIST, LFSR, Xilinx, Linear feedback shift register, MISR, Multiplier, VHDL

I. INTRODUTION

Microelectronics circuits now operate in nanometer regions. The SOC(System on chip) has become highly sensitive to faults, these faults produce undesirable results which can lead to failure of a chip. Various types of defects introduced during manufacturing. Even a small defect in a single IC can bring down the whole system to standstill. Sometimes the faults are very tricky to find, Hence thorough testing of the IC is very essential. Hence, the job of finding out the functionality of a circuit is highly complex. Also it is time consuming. If a bad or damaged chip passes an improperly designed Testing algorithm, the whole system can crash and the task of debugging becomes impossible .

The faults in system are more complicated at system level then at board level . Therefore debugging of faults should be carried out early. Today's ICs have a very high transistor density. More than 10^9 (1 Billion) transistors are ingrained in a single IC chip. It necessary to ensure the proper functionality of ICs that too in a limited time.DFT techniques have gained more importance.

Traditionally ATEs are used to test IC chips, But ATEs are very costly, Bulky and non movable, also they do not provide full accessibility to circuit's internal nodes .BIST can be seen as a alternate for ATE. It is cheap and provides fast testing; Also its power consumption is low. Thus BIST is being extensively used for testing of memory elements and various combinational circuits.

II . BIST ARCHITECTURE

BIST is a DFT methodology in which testing is done without using external or extra testing hardware, All testing is done with an on-chip specialized testing mechanism .Advantage of using BIST is that test patterns/vectors are generated by onboard testing circuit, Hence costly external ATEs are not required. It saves the memory requirement during test. A typical BIST structure consists of a TPG, Counters, ROM, LFSR are used as TPGs. MISR is generally used to analyses the test responses (TRA). BIST control unit (BCU) [1], which switches from testing mode to normal mode this approach allows Field testing of circuits and eradicates the necessity for a external testing circuit.

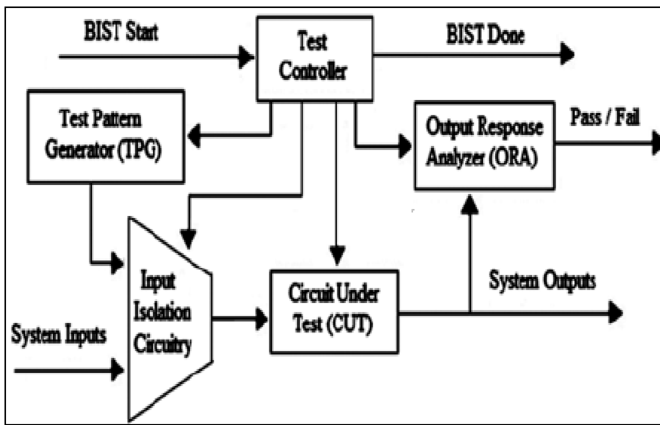

Figure 1: Basic block diagram of a BIST

• Test pattern Generator : It creates the test patterns/vectors for CUT. It can be implemented as a standalone circuit[2]. Various techniques for pattern generation such as deterministic, random or Pseudo random are used. But it is seen that using pseudorandom and random generators results in faster convergence towards a fault. Hence LFSR is used as a TPG. The input of LFSR is linear function of its preceding state. It is made up of D flip-flips and linear XOR gates. A properly designed LFSR can cycle through 2^n-1 unique states[7]. Pseudo random sequence generator is created in HDL as per the circuit shown in following Figure 2.

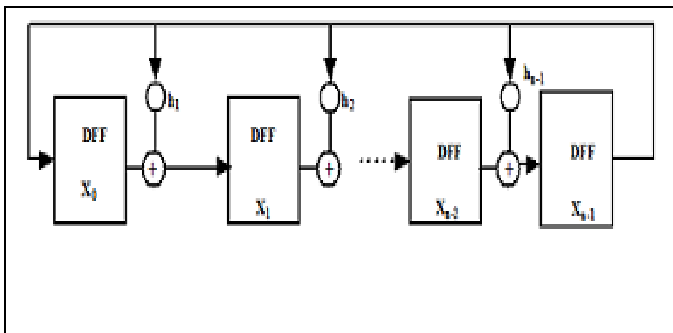

Figure 2: Modular LFSR

• Circuit under Test: Also called Device under test is part of the circuit tested using BIST. Sequential, combinational or a memory is the most common circuits used as CUT for BIST .Here CUT is 4 bit Multiplier. Multiplier can be made using various algorithms/ techniques like array, booth, column bypass and Wallace tree[5] .Among this array multipliers have the most primitive architecture. It is mainly used in small circuits. Its hardware requirement is less but speed of operation is slow. Here we have created a gate level structure of multiplier .Half adder, Full adders and AND gate are used in its implementation [3]. This is the most basic design of a multiplier.

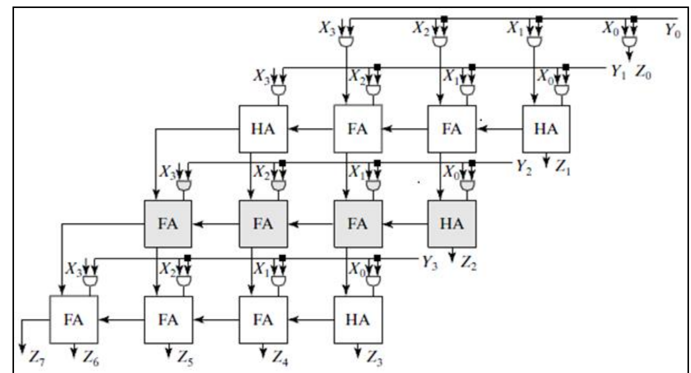

Figure 3: 4 Bit Multiplier

• Test Response Analyzer (TRA): It evaluates the sequence on primary output and matches it with the golden signature or expected output. If LFSR are used for response analysis then the hardware requirement is very large. A MISR reduces the hardware by compressing the multiple bit streams. Therefore a MISR is used instead of using multiple parallel LFSRs. We can synchronize the Test patterns for BIST with LFSR by using a common clock pulse .The outputs of the CUT are then correlated with an expected response which is also called golden signature. Signature analysis is efficient and widely used compaction technique. MISR compacts all outputs in a single LFSR. LFSR is linear, Also it complies with superposition principle[10]. Its output creates a signature depending on the action of all the bits fed into it. If any bits are wrong or different, the signature will be distinct from the expected value and a fault will have been detected. Only drawback of MISR is that they are susceptible to signature error cancellation and aliasing.

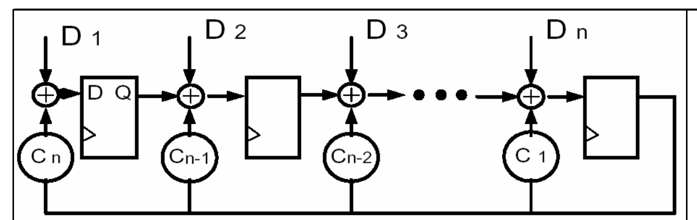

Figure 4: Generalized MISR

• BIST control unit: It regulates and supervises the test execution operation; it supervises the TPG, CUT, TRA and configures the CUT. It is turn on by the normal/test signal.

• Input MUX:It is used to switch from normal operating mode to testing mode. In testing mode input vectors are provided by the LFSR.Thus it controls whether the input is from user or LFSR.

III. Simulation and Synthesis Results

The BIST based Multiplier design is created using VHDL Vivado. The RTL of the proposed design is as in Figure 7. The simulation of the complete design is carried on Xilinx Vivado Tool using VHDL Test Bench. The simulation waveform result of the BIST-multiplier and the multiplier designs are as in Figure 8 and Figure 9 respectively.

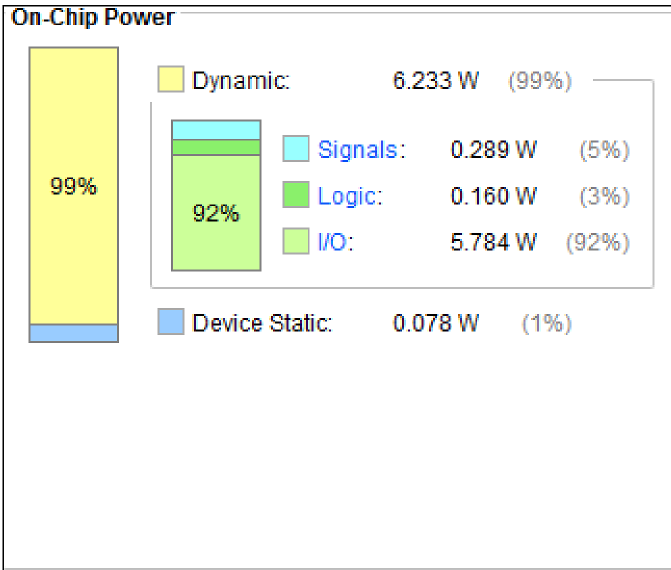

Figure 5: Power consumption (Fault Free Circuit)

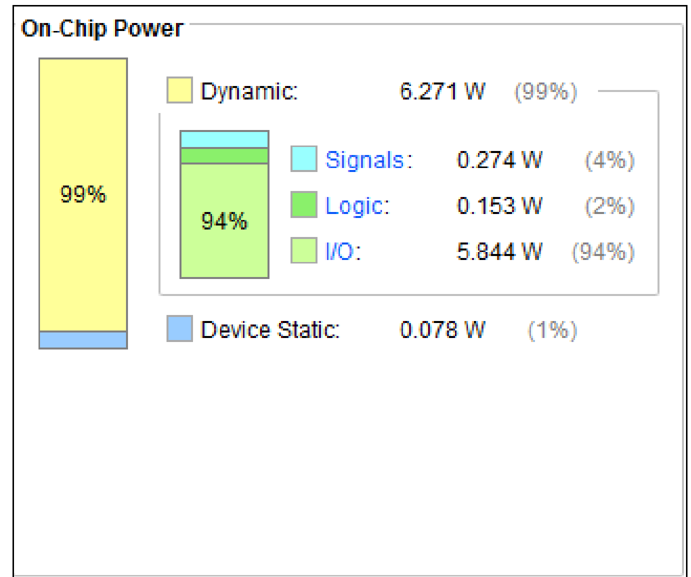

Figure 6: Power consumption (Faulty Circuit)

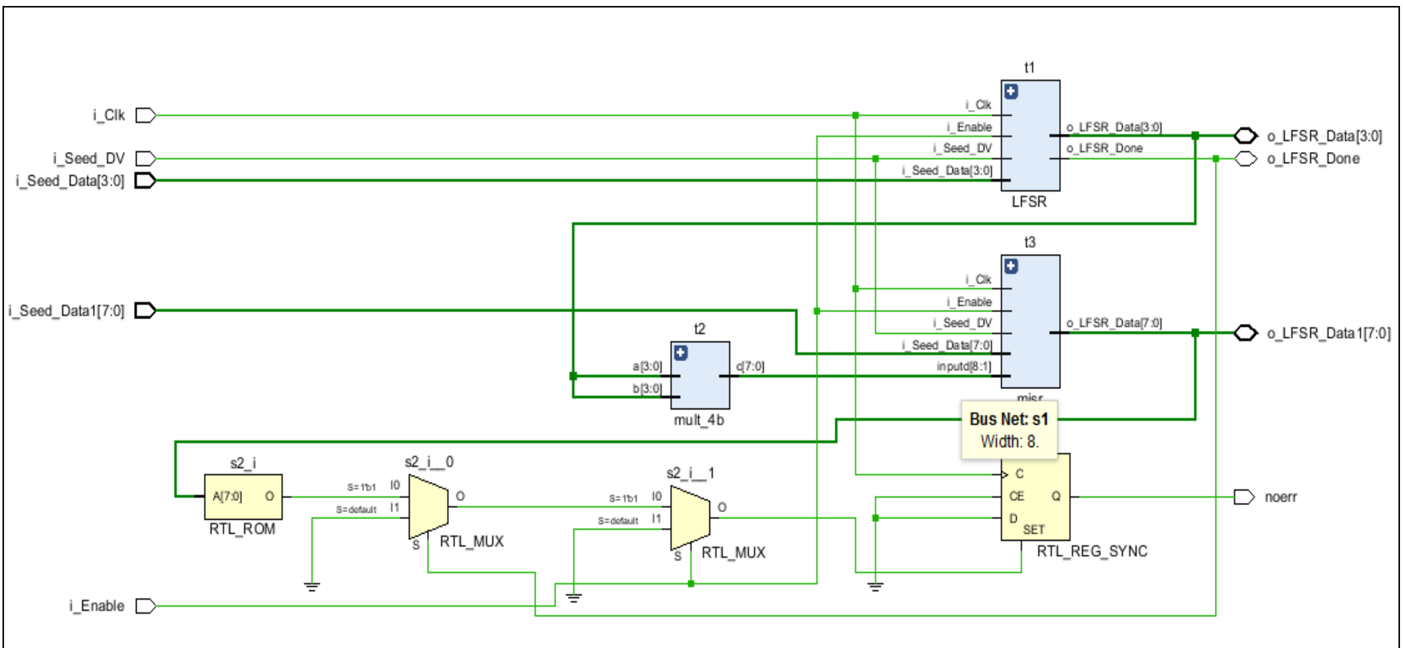

Figure 7: RTL View of BIST structure

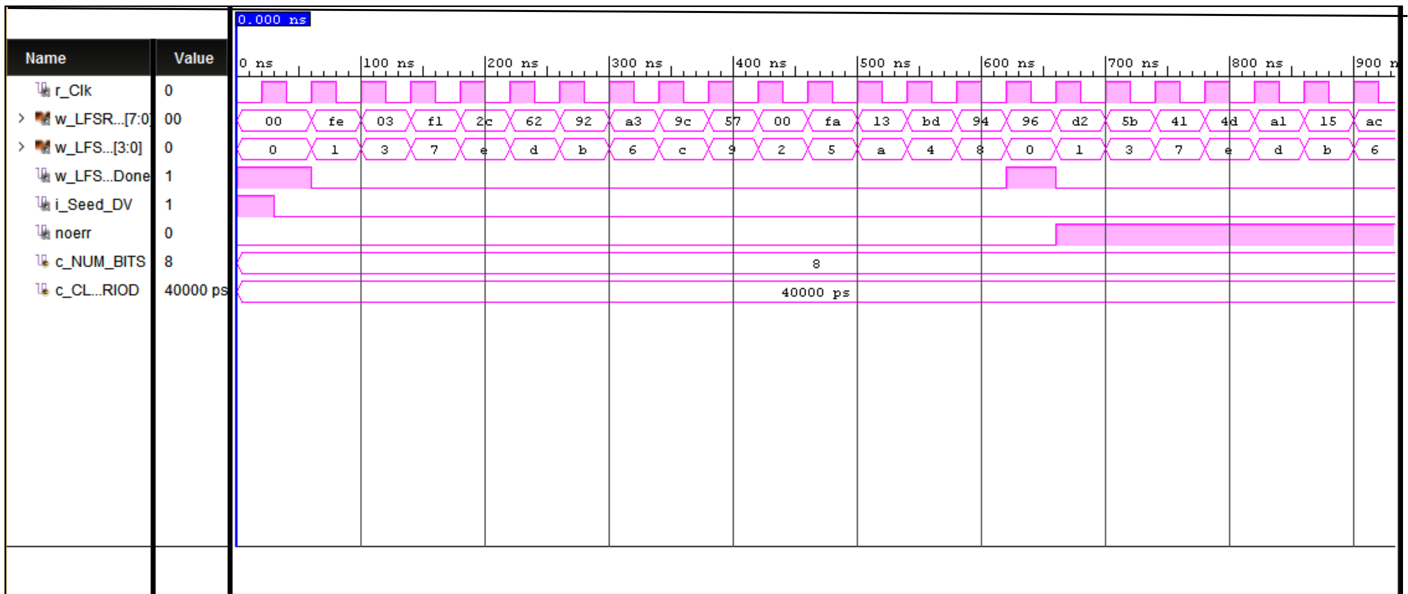

Figure 4: Figure 8: Simulation of a fault free circuit (Noerr='1')

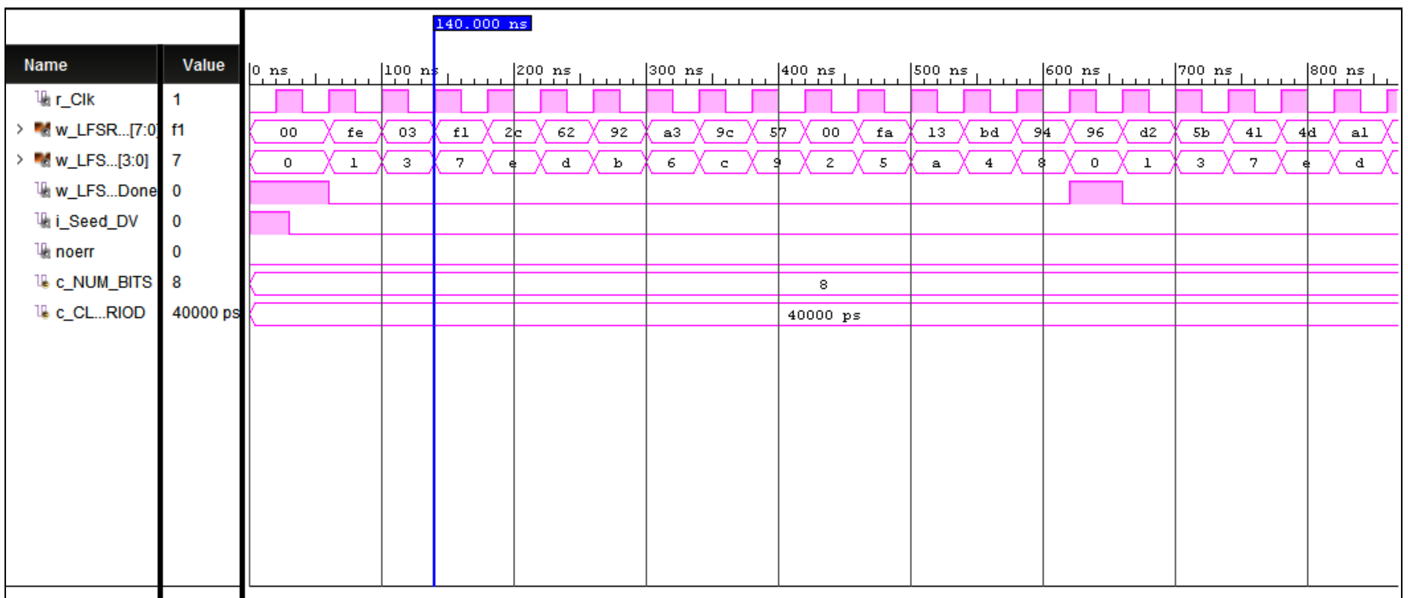

Figure 9: Simulation of a faulty circuit (Noerr='0')

IV.CONCLUSION

This an entry level project on BIST based Multiplier design, there is tremendous scope for further improvements. We have successfully impended a BIST based Multiplier, with on-chip verification. Using BIST the time for testing is reduced significantly, also BIST is a cost effective solution compared to ATE. Implementing BIST increases the hardware overhead of the circuit, this is one of the disadvantages of BIST

REFERENCES

[1] Nagaraj S Vannal "DESIGN AND TESTING OF COMBINATIONAL LOGIC CIRCUITS USING BUILT IN SELF TEST SCHEME FOR FPGAs" 2015 Fifth International Conference on Communication Systems and Network Technologies

[2Bharti Mishra , Dr. Rita Jain and Prof. Richa Saraswat " Low Power BIST based Multiplier Design and Simulation using FPGA ",2016 IEEE Students' Conference on Electrical, Electronics and Computer Science

[3] Nishant Govindrao Pandharpurkar* and V. Ravi " Design of BIST using Self-Checking Circuits for Multipliers" Indian Journal of Science and Technology, *Vol 8(19), DOI:10.17485/ijst/2015/v8i19/77006, August 2015*

[4] M.H. Husin, S.Y. Leong, M.F.M. Sabri, R. Nordiana "Built in self test for RAM Using VHDL "2012 IEEE Colloquium on Humanities, Science & Engineering Research (CHUSER 2012), December 3-4, 2012, Kota Kinabalu, Sabah, Malaysia 272

[5] Designing of BIST Architecture of Generic Multipliers.Anju Rajput, *IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) Volume 4, Issue 5, Ver. II (Sep-Oct. 2014)*

[6] Pushpraj Singh Tanwar, Priyanka Shrivastava ," VHDL Implementation of Logic BIST (Built In Self Test) Architecture for Multiplier Circuit for High Test Coverage in VLSI Chips "International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering [7] Essays, UK. (November 2013). Built In Self Test Computer Science Essay. Retrieved from http://www.ukessays.com/essays/computerscience/ built-in-self-test-computer-science-essay.php?cref=1

[7] ESSENTIALS OF ELECTRONIC TESTING FOR DIGITAL, MEMORYAND MIXED-SIGNAL VLSI CIRCUITS,BUSHNELL, M., AGRAWAL, VISHWANI

[9] HTTP://EN.WIKIPEDIA.ORG/WIKI/LINEAR_FEEDBACK_SHIFT_REGISTER

[10] TESTING OF EMBEDDED SYSTEM VERSION 2 EE IIT, KHARAGPUR

[11] HTTP://IROI.SEU.EDU.CN/BOOKS/ASICS/BOOK2/CH14/CH14.7.HTM [12] HTTP://WWW.ENGINEERSGARAGE.COM/CONTRIBUTION/POWER-OPTIMIZATION-OFLFSR? PAGE=2

[12]http://www.slideshare.net/ijsrneteditorial/implementation-of-lowpower-
test-pattern-generatorusing-lfsr