Reconfigurable Ultra Low Power LNA With and Without in Band Interference Rejection for IoT Application

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Abstract - **In this paper, a reconfigurable Ultra low power Low Noise Amplifier (LNA) is presented. In this work,subthreshold driven Common Gate (CG) input stage is modified to provide wideband input matchingand a current reuse noise cancelling technique is introduced toimprove noise performance. Additionally, substantial reductionin power consumption is obtained by driving the MOS devices insubthreshold region. To provide dual output i.e. with and without Interference Rejection a High Isolation and Low Insertion Loss SPDT Switch is used. Negative Gm Based LC Series Notch Filter is used for the interference rejection. This Circuit achieved a gain of 10 dB (1 dB) with NF 6.3-7.2 over the bandwidth of 1.5-5.5 GHz in one port and 35dB Inference rejection of Narrow band @2.45GHz, A very high Isolation is obtained between the two ports i.e. 54dB. This is suitable for IOT Wireless Sensor Nodes. The circuit is simulated in Cadence Virtuoso using Spice Models in TSMC 65nm node.**

Index Terms –Ultra-Low Power LNA, SPDT Switch, Notch Filter.

I. INTRODUCTION

With the advent of the internet of things, the demand of the ultra-low power system has increased. We need to have low power sensor node since the frequent change of the battery is not possible. It is expected to have 30 billion devices connected by 2020 through IOT [1]. The received signal strength for the UWB is much lower than the narrow band. This paper presents an ultra-low power reconfigurable LNA with dual ports. Port 1 provides the direct LNA output and the other port provides an output with the notch @2.45GHz.
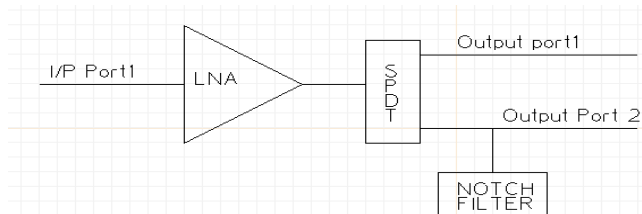

Fig 1. LNA Integrated with SPDT Switch and Notch Filter

This paper is organized as follows: after a brief introductionin Section I, Section II presents LNA design in detail. SPDT Switch and Notch Filter employed in this paper is discussed briefly in Section III and IV. Similarly, the simulation results are presented in section V, and finally this paper wraps with a brief conclusion at section V. This paper is organized as follows: after a brief introduction.

II. ULTRA – LOW POWER LNA

The LNA Presented here is a two stage LNA. First Stage of LNA is the CG stage and the second stage is the current reused CS-CG stage with current reused, gain boosted and feed forward noise cancellation. Transistor are operated in the subthreshold regime to reduce the power consumption.

Parameter/Year	This work	2017[1]	2016[2]
BW(GHz)	1.5-5.5	2-5	0.6-4.2
AV(dB)	19	13	10-14
S11(dB)	<-10	<-10	12-13.2

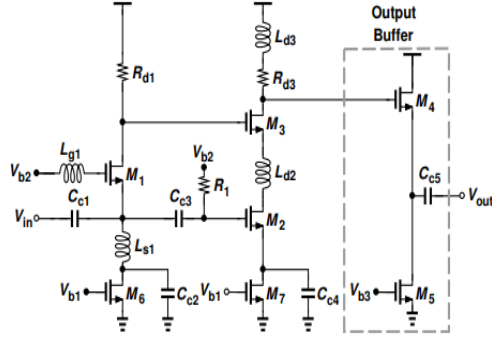| NF(dB)	6.3-7.3	6-8	<-10
CP1dB (dBm)	-21	-15	-20
VDD(v)	1.2	1.8	0.5
PDC(mW)	1.44	1.8	0.25
Tech(nm)	65	65	130

Table 1： Comparison with other works

Fig 2．LNA with Buffer

CG input stage is modified to achieve the wide band input matching. To get the 50–ohm matching in the input stage gm of the input transistor should be 20 mS． Device sizes must be very large to achieve gm=20ms which will increase the cgs and hence reduce the bandwidth．To solve this problem inductor is introduced in the input of CG stage ［1］．The gate inductor reduces the effect of gm as it resonates with the cgs and moves its effect to higher frequencies．

$$Z_{in} = Z_{S1} \| \frac{1}{g_{m1}(1-\alpha)} \| \frac{1}{sC_{gs1}(1-\alpha)} \quad (1)$$

$$\alpha = \frac{sC_{gs1}p + sC_{gd1}g_{m1}}{p \cdot q + sC_{gd1}(g_{m1} - sC_{gd1})},$$

Here, $p = (1/ZL1 + sCgd1)$, $q = (1/ZG1 + sCgs1 + sCgd1)$,
and $ZG1 = (sLg1 + RLg1) \| (1/sCgb1)$.
S11 is the parameter used to assess the input matching shown in fig 3 as $S11 = |Zin-Zs|/|Zin+Zs|$．This LNA achieve S11 <-10 in the frequency range of 1．5 GHz to 5．5 GHz．
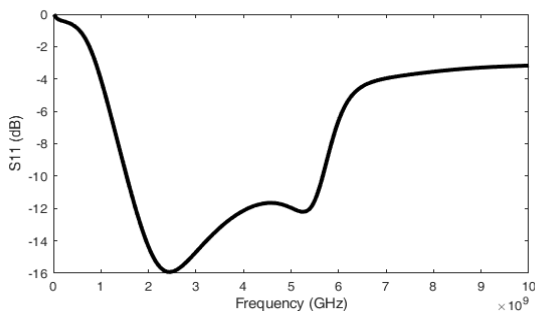

Fig 3. S11

The simulated stability factor, Kf, is shown in Fig．5．Since, Kf> 1 from 1 GHz to 10 GHz, the LNA is unconditionally stable.

The gain of the LNA can be calculated as the gain of first stage and the gain of current reused gain boosted CS CG Stage．

$$Av = Av1.Av3 + Av2 \quad (2)$$

WhereAv1=gm1ZL1．AndAv2=(gm2/(1+sZs3Cdb2))(gm3ZL3/(gm3+sCsb3+sCgs3)),Av3=(gm3ZL3/(1+gm3Zgen3))．Here gm=transconductance of coresponding stage, ZL is load impedance, Cgs is gate to source capacitance, Csb is source to body capacitance．
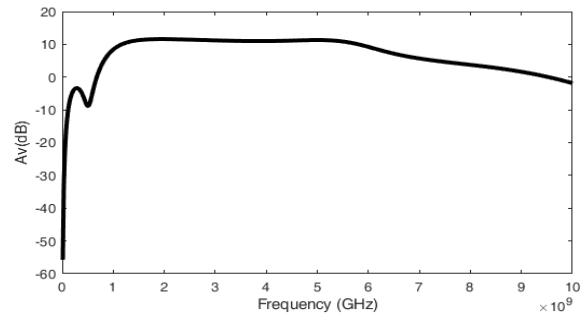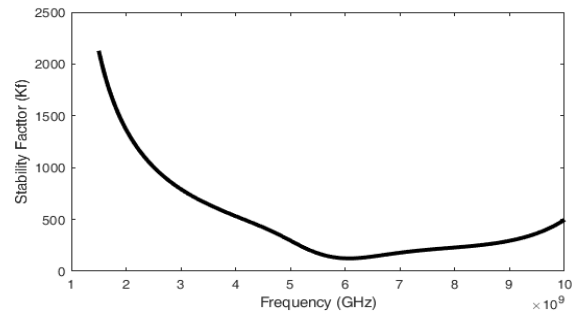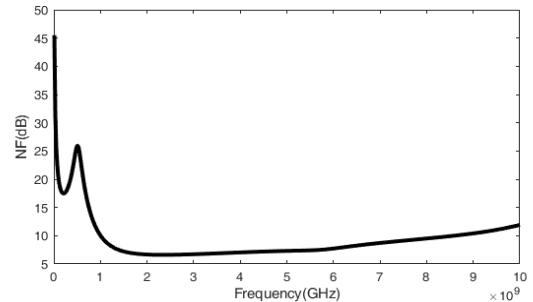

Fig.4 Gain

Fig 5．Stability Factor

Fig 6. Noise Figure

III.   SPDT Sᴡɪᴛᴄʜ

Various Switch Topologies that can be used for the design of the SPDT (Single Pole Double Throw) Switch. The Simplest and compact among all is a simple Series Switch Fig 7 (a). However, this usually does not provide enough Isolation in the off port unless we have customized layout techniques utilizing

increased drain source region. To improve the Isolation, one of the popular solution is to append Shunt transistor in the present structure Fig 7 (b). This approach increases the off-portIsolation, but the Off-State shunt transistors is connected to ground, so the gate has to be biased below zero volts, in order to improve power-handling capability, which is an undesirable issue. Fig. 7(c) by adding the bypass capacitors PHC can be improved without using negative biasing for the off-state transistors.This work presents a Series Shunt SPDT switchdesigned using NMOS Transistor with bypass capacitors to avoid negative biasing supply. The body floating resistors are usedto further enhance the power handling capacity of the switch. The series nmos have the main switching function and the shunt NMOS are used to increase the isolation among the ports. It is observed that the sizes of the series and shunt MOSplays an important role in the performance of the switch especially the Isolation and PHC. We can use the large shunt NMOS sizes and small series NMOS or the other way around like small shunt sizes and large series sizes, in both cases the Insertion loss remain the same but the Isolation and PHC are the crucial factors. During the on state, if the series NMOS sizes are large then they can uphold large maximum current and hence improve the PHC. In the offstates if the shunt NMOS are of small sizes, then the draw less negative current hence increases the Isolation. This

implies that in a SPDT Switch design there is a trade-off between the Isolation, PHC and Insertion loss based on device sizes.

Parameter/ Year	This Work	2006[5]	2015[10]
Frequency (GHz)	4(0-22)	5.8	5
Insertion Loss (dB)	1.0	1.1	1.1
Isolation(dB)	54	27	40
Input Return Loss(dB)	-	13.2	-
CP1dB	11.29	20	21.0
Switch type	Series-shunt switch	Series-shunt with body floating	Back Gate and Floating Bias

Table 2: SPDT Switch Comparison with other work

With Transmission Gate

Parameter	With Floating Resistor		Without Floating Resistor	
VC	1.2	1.2	1.2	1.2
VC_BAR	−1.2	0	−1.2	0
Isolation	42	41.41	40	39
P1dB Compression Point	11.01	4.07	6.9	3.484
BW) 3dB (	22.66	23.34	16.9	16.89

Table 3

Without Transmission Gate (only NMOS)

Parameter	With Floating Resistor		Without Floating Resistor	
VC	1.2	1.2	1.2	1.2
VC_BAR	−1.2	0	−1.2	0
Isolation	50	48	54	54
P1dB Compression Point	6.07	3.21	4.94	3.04
BW) 3dB (	43	45	31	30.4

Table 4

From the above table 3&4 we can conclude that design of SPDT Switch with only NMOS and without body floating technique must be used since this design major concern is Isolation rather than the 1 dB compression point. Both Biasing technique provide same isolation, so we prefer the biasing technique with VC=1.2 V and VC_BAR = 0V since it is easier to implement.
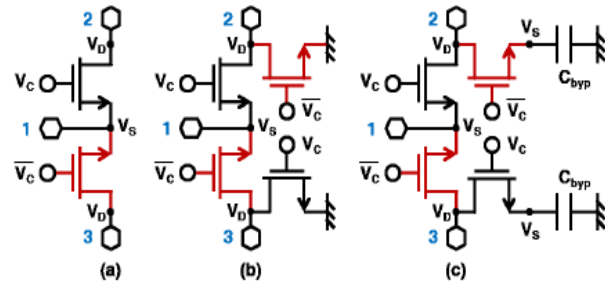

Fig 7: Biasing technique.

Prototype presented in this work is designed using the TSMC65nm node and the device sizes are optimized to get desired results considering the trade-off among various parameters. The length of each transistor is fixed at 60nm and the width are as follows M1=2uM2=1uThe achieved

isolation is greater than 54dB with the insertion loss of 1dB and the 1dB Compression point being 3.04dB.

IV. NOTCH FILTER

One of the main challenges for the design of LNA is the ability of the circuit to reject the interference at 2.4 GHz Range. Previous literatures have also addressed this issue [2][7][8], but unable to achieve strong rejection in this region [5][6]. The depth of the notch (attenuation at a desired frequency) is directly related to the quality of the filter circuit. Inductors that can be manufactured in the current CMOS technology havevery low-quality factor, which impedes in gaining a good quality filter.

$$Q = \omega L/R \qquad (1)$$

As evident from (1) to obtain high value of Q, R needs to be cancelled. The basic idea of using a Q-enhanced technique is produce negative resistance, to compensate the losses of the LC circuit and then boost the Q of the lossy circuit. Two back-to-back connected (cross-coupled) MOS transistors can generate negative resistance. Once the negative resistance is tuned to be equal to the resonator losses, which is dominated by the loss of the inductor- then the losses can be compensated, and a perfect notch filter is obtained. Care should be taken that complete elimination of R by negative resistance of gm cells leads to the oscillation of the circuit and render unstable.

The Notch Filter that has been designed in this circuit is composed of a series LC circuit that presents very small impedance at resonance frequency. The cut off frequency for this filter is chosen to be around 2.45 GHz, to obtain the attenuation in the region. The value of negative resistance is tuned around this range to obtain a lossless resonator circuit. At the frequency of interest for attenuation, the output current is steered away from the load by the perfect notch filter instead of being converted into voltage at the load of the circuit. This leads to signal attenuation at this frequency range and hence produce a notch in the gain (S21) of the LNA.
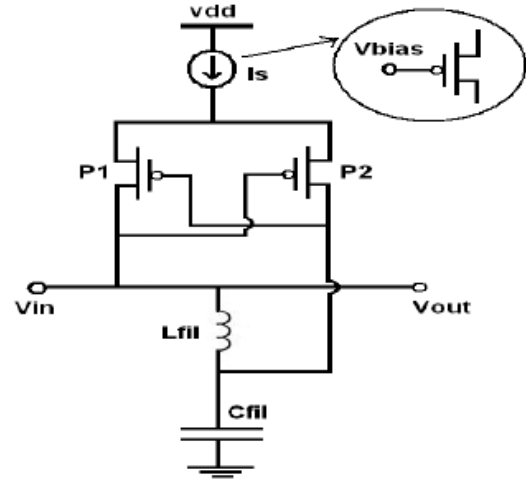

Fig 8. Notch Filter Circuit (with negative gm)

The negative resistance is synthesized by the cross-coupledPMOS transistors P1 & P2, biased by current source Is, which is realized by a single pMOS transistor of size 1um and length 100 nm. The twoTransistors P1-P2 have an identical size of 112um and length 100nm. The gate of P1 which is connected to the drain of P2, is in turn connectedto one end of L, while its drain terminal connected to the gate of P2, is in turn connected to the other terminal of L. This kind of structure known as cross-coupled configuration generatesthe required negative resistance between the MOSFET drains, which is responsible for cancelling the on-chip resistance of L.

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{2}{sC_{gs} - g_m} = -2\frac{g_m + sC_{gs}}{g_m^2\left(1 + \frac{\omega^2}{\omega_T^2}\right)}$$

$$= \frac{-2}{\left(1 + \frac{\omega^2}{\omega_T^2}\right)}\left(\frac{1}{g_m} + j\frac{\omega}{\omega_T}\right)$$

$$= R_{in} = RE(Z_{in}) = RE\left\{\frac{-2}{\left(1 + \frac{\omega^2}{\omega_T^2}\right)}\left(\frac{1}{g_m} + j\frac{\omega}{\omega_T}\right)\right\} \Rightarrow -\frac{2}{g_m}$$

For the matched MOSFETs, the resistance between the two drain terminals is −2/gm. Hence, the term *negative gm circuit*.
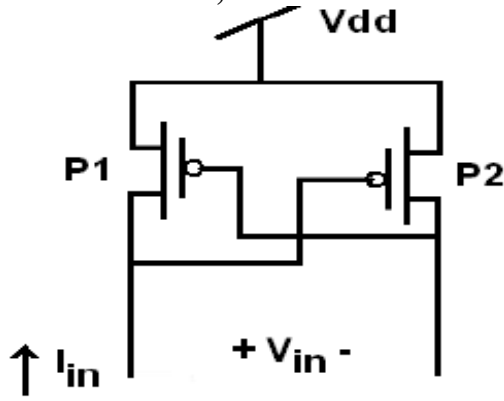
Fig 9. Analysis of Negative Resistance of cross-coupledtransistors. The Neg resistance is between the MOSFET drains.

V Results

The simulation results are as follows. Fig 10 and Fig 11 shows gain and Isolation when the port 2 is on and Fig 12 and Fig 13 shows gain and Isolation when port 1 is on.
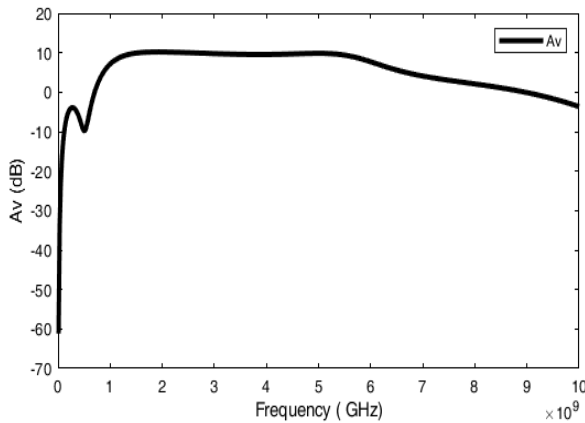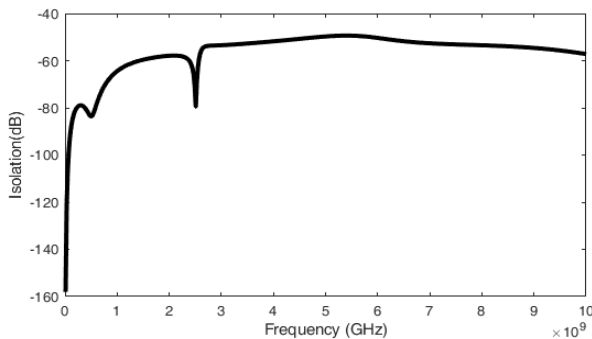

Fig 10. Av (Without Notch)Port 2

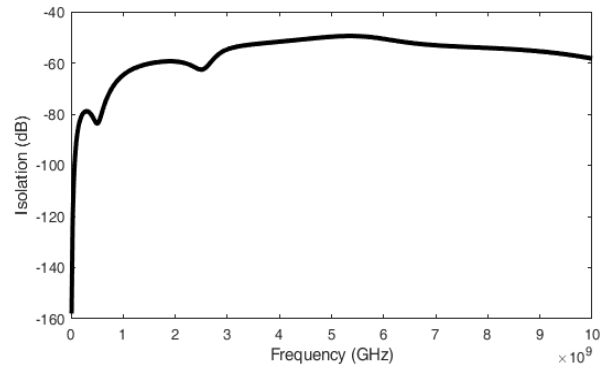Fig 11. Isolation between port 2 and port3 when port 2 is on

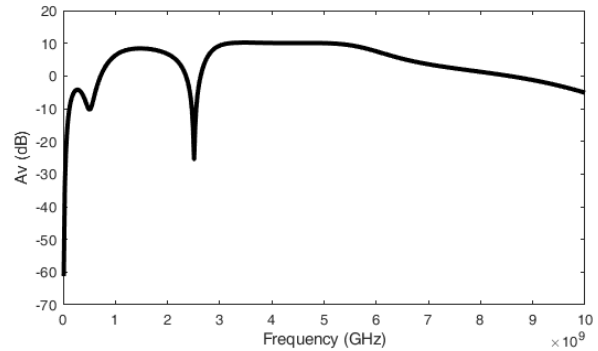Fig 11. Isolation between port3 and port2 when port 3 is on

Fig 10. Av (with Notch) @ Port 3

CONCLUSION

This Paper presents an ultra-low power LNA integrated with the SPDT Switch and Notch Filters. Whole system consumes 3.8 mili watts and a gain of around 10 dB with very high isolation between two ports i.e..54 decibels (min) over the bandwidth of 1.5−5GHz. The system is suitable for low power wireless sensor nodes used in IOT.

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